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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
03-0861 (81580)	

Application Number	Filed
10/650,296	8/27/03

First Named Inventor	
Tetelbaum	

Art Unit	Examiner
2825	SIEK, VUTHE

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 38,657
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

Eric J. Whitesell
Typed or printed name

858-552-1311
Telephone number

November 14, 2005
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

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DOCKET NO. 03-0861
81580(6653)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: TETELBAUM, Alexander

Serial No.: 10/650,296

Filed: August 27, 2003

For: METHOD OF CLOCK DRIVEN CELL PLACEMENT AND CLOCK TREE SYNTHESIS FOR INTEGRATED CIRCUIT DESIGN

Art Unit: 2825

Examiner: Siek, Vuthe

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below.

November 14, 2005 Julie Freiburger

BRIEF IN SUPPORT OF PRE-APPEAL REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the final Office Action mailed on October 19, 2005, please enter the following brief in support of the attached Pre-appeal Request for Review. A Notice of Appeal is also submitted herewith.

ARGUMENTS

Claims 1-2, 5-11, and 14-18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lu et al., U.S. Patent 6,550,045 (*Lu*). Claims 1 and 10 recite steps of identifying critical paths in an integrated circuit design, partitioning the integrated circuit design into a timing group for each of the critical paths wherein each timing group includes only critical paths, assigning each flip-flop in a critical path to a timing group corresponding to the critical path, performing a cell placement to minimize a function of propagation delay and maximum distance between flip-flops within each timing group, and constructing a clock sub-net for each timing group.

The rejection errs in assuming a definition of critical path that is not the same as the claimed critical path

Regarding Claims 1 and 10, the rejection alleges in section 5 on page 2-3 that the summary and column 4 in *Lu* teach the claimed step of identifying critical paths in the integrated circuit design. However, the rejection errs in substituting its own definition of a critical path as "a data logic path having timing information affecting network timing, timing violations" in place of the claimed critical path defined in the specification. As explained on page 12, line 18 to page 13, line 2 of the specification, "a path is critical to the setup time requirement if the propagation delay of the path is more than an empirical threshold, typically about 90 percent, of the clock period" and "a path is critical to hold time if the propagation delay of the path is less than an empirical threshold, typically about 10 percent, of the clock period". Because the rejection assumes a definition of a critical path that is not the same as the definition in the specification of the claimed critical path, the assumed critical path is not identical to the claimed critical path. Because the

assumed critical path is not identical to the claimed critical path, the rejection does not meet the burden required to show anticipation under 35 U.S.C. § 102.

The rejection errs in concluding that *Lu* teaches the claimed timing groups

The rejection further alleges that *Lu* teaches "partitioning the integrated circuit design into a timing group" in the summary; column 3-4; and FIGS. 1 and 6. However, the rejection errs in alleging that FIG. 1 shows two groups of critical paths. For example, the rejection alleges that the path in FIG. 1 from the clock source (10) to the flip-flop (20) and through the logic (30) to the flip-flop (22) is a group of critical paths. However, the path described by the rejection is clearly a single path, not a group of paths as alleged by the rejection. Similarly, the path described by the rejection from the clock source (10) to the flip-flop (22) and through the logic (32) to the flip-flop (24) is clearly a single path, not a group of paths as alleged by the rejection. Further, even if the assumed definition of a critical path were correct, neither FIG. 1, FIG. 6, nor the accompanying descriptions support the allegation that each of the paths cited by the rejection necessarily includes a timing violation "that needs to be fixed" as alleged by the rejection. Also, Lu does not teach that the paths are partitioned into groups as alleged by the rejection.

Because the single paths cited by the rejection do not each constitute a group of critical paths as alleged by the rejection, and because Lu does not teach partitioning the IC design into timing groups, the rejection fails to show that *Lu* discloses the claimed step of partitioning the integrated circuit design into a timing group for each critical path. Because the rejection fails to show that *Lu* discloses the claimed step of partitioning the integrated circuit design into a timing group for each critical

path, the rejection fails to meet the burden required to show anticipation under 35 U.S.C. § 102.

Even if both paths did include a timing violation, they could not belong to two different timing groups as alleged by the rejection, because the flip-flops (20), (22) and (24) clearly communicate with each other through the data logic (30) and (32). As defined in the specification on page 15, lines 11-19, the claimed timing groups require that flip-flops in one timing group do not communicate with flip-flops in another timing group. Because the flip-flops cited by the rejection cannot belong to different timing groups, the rejection fails to meet the burden required to show anticipation under 35 U.S.C. § 102.

The rejection errs in assuming that assigning each flip-flop to a critical path is identical to assigning each flip-flop in a critical path to a timing group corresponding to the critical path

The rejection further alleges that *Lu* teaches "assigning each flip-flop to a critical path" in FIGS. 1, 6. However, Claims 1 and 10 do not recite assigning each flip-flop to a critical path. Claims 1 and 10 recite assigning each flip-flop in a critical path to a timing group corresponding to the critical path. Even if *Lu* did teach assigning each flip-flop to a critical path as alleged by the rejection, the alleged teaching in *Lu* is not identical to the step recited in Claims 1 and 10. Because the alleged teaching in *Lu* is not identical to the step recited in Claims 1 and 10, the rejection fails to meet the burden required to show anticipation under 35 U.S.C. § 102(e).

The rejection errs in concluding that Lu teaches minimizing a function within each timing group

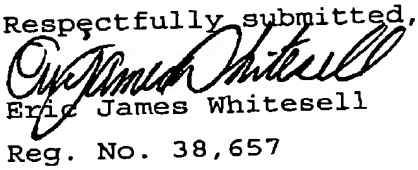
The rejection further alleges that FIGS. 1, 6, their descriptions, and column 6 in *Lu* teach performing a cell placement

to minimize a function of propagation delay and maximum distance between flip-flops within each timing group as recited in Claims 1 and 10. However, the rejection lacks the claimed timing group as explained above. Because the rejection lacks the claimed timing group as defined in the specification, the rejection fails to meet the burden required to show anticipation under 35 U.S.C. § 102.

The rejection errs in concluding that "substantially similar" meets the burden required under 35 U.S.C. § 102

Regarding Claims 2, 5-9, 11 and 14-18, the rejection further alleges in section 6 on page 3 that FIGS. 1 and 6 in *Lu* teach limitations that are "substantially similar" to those recited in Claims 2, 5-9, 11 and 14-18. However, to show anticipation under 35 U.S.C. § 102, the prior art must teach limitations that are identical to those claimed, not merely similar. Because the rejection applies limitations that are merely similar rather than identical to the claimed limitations, the rejection does not meet the burden required to show anticipation under 35 U.S.C. § 102.

Respectfully submitted,



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